associated with the grant, modified as necessary by the rate control command on the F-RCCH.

FIG. **11** depicts timing for an example embodiment with combined acknowledgement and rate control channels, along with a new grant. A request, grant, subpacket transmission (not decoded correctly) and NAK are transmitted the same as the first eight frames described above with respect to FIG. **10**. In this example, the second subpacket transmission is also received and decoded correctly. However, instead of an ACK_RC being sent by the base station, an ACK_STOP is transmitted. If no grant accompanied the ACK_STOP, the mobile station would revert to autonomous transmission. Instead, a new grant is transmitted. The mobile station needn't monitor the F-RCCH for this frame. The mobile station then transmits the first subpacket of the next packet in accordance with the new grant.

FIG. **12** depicts timing for an example embodiment with combined acknowledgement and rate control channels, without a grant. This example is identical to FIG. **10**, except that no grant is sent in response to the original mobile station request. Thus, the first subpacket transmission of the first packet is transmitted at the autonomous rate. Again, this subpacket is decoded incorrectly at the base station. The second subpacket is again decoded correctly, and an ACK_RC is transmitted along with a rate control command. The mobile station then sends the next packet at the potentially adjusted rate. This example illustrates the possibility of moving a mobile station rate arbitrarily using rate control commands only, without any grant.

Note that in an alternative embodiment, a base station may use rate control with autonomous transmissions with or without a previous request. Reductions may be used to relieve congestion, and an increase may be awarded when there is extra capacity, even though the BS may not know the data requirements, since a request was not transmitted.

It should be noted that in all the embodiments described above, method steps can be interchanged without departing from the scope of the invention. The descriptions disclosed herein have in many cases referred to signals, parameters, and procedures associated with a 1xEV-DV system, but the scope of the present invention is not limited as such. Those of skill in the art will readily apply the principles herein to various other communication systems. These and other modifications will be apparent to those of ordinary skill in the art.

Those of skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

Those of skill would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. An apparatus, comprising:
a message generator configured to:
generate a first message comprising an acknowledgment indicator and a rate control indicator, wherein the rate control indicator indicates at least whether a rate control command will be generated and issued; and
generate a second message conditioned on the rate control indicator indicating at least that the rate control command will be generated and issued.

2. The apparatus of claim **1**, wherein the second message comprises the rate control command.

3. The apparatus of claim **2**, wherein the rate control command is one of a plurality of values, wherein one or more of the plurality of values indicates a rate increase.

4. The apparatus of claim **2**, wherein the rate control command is one of a plurality of values, wherein one or more of the plurality of values indicates a rate decrease.

5. The apparatus of claim **2**, wherein the rate control command is one of a plurality of values, wherein one or more of the plurality of values indicates a rate hold.

6. An apparatus, comprising:
a receiver configured to receive a packet;
a decoder configured to decode the received packet; and
a message generator configured to: